What is claimed is:

1. A method for detecting semiconductor process stress-induced defects comprising:

providing a polysilicon-bounded test diode, said polysilicon-bounded test diode comprising a diffused first region formed in an upper portion of a second region of a silicon substrate, said second region of an opposite dopant type from said diffused first region, said diffused first region surrounded by a peripheral dielectric isolation and a peripheral polysilicon gate comprising a polysilicon layer over a dielectric layer, said polysilicon gate overlapping a peripheral portion of said diffused first region;

stressing said polysilicon-bounded test diode; and

monitoring said stressed polysilicon-bounded test diode for spikes in gate current during said stress.

2. The method of claim 1, wherein said step of stressing comprises:

maintaining said polysilicon-bounded test diode at an elevated temperature;

applying ground potential to said polysilicon gate, said second region and said silicon substrate; and

applying a reverse bias ramping voltage to between said first and second regions.

3. The method of claim 1, wherein

said diffused first region has a length of 50 to 100 microns and a width of 2 to 10 microns;

said polysilicon gate has a width of 0.5 to 1.5 microns; and

said polysilicon gate overlaps said first diffused region by 0.1 to 0.6 microns.

4. The method of claim 2, wherein said ground potential is zero volts and said ramping voltage is ramped from 0 to -6 volts and said elevated temperature is 100 to 200 °C.

5. A method for detecting semiconductor process stress-induced defects comprising:

providing one or more polysilicon-bounded test diodes, each polysilicon-bounded test diode comprising a diffused first region within an upper portion of a second region of a silicon substrate, said second region of an opposite dopant type from said diffused first region, said diffused first region surrounded by a peripheral dielectric isolation and a peripheral polysilicon gate comprising a polysilicon layer over a dielectric layer, said polysilicon gate overlapping a peripheral portion of said diffused first region;

stressing each said polysilicon-bounded test diode;

measuring during said stressing, for each said polysilicon-bounded test diode, a current through said first region as a function of a forward bias voltage applied between said first and second regions at at least a predetermined forward bias voltage; and

determining the frequency distribution of the slope of said forward bias voltage versus said first region current at said pre-selected forward bias voltage for said one or more polysilicon-bounded test diodes.

6. The method of claim 5, wherein said step of stressing comprises:

applying ground potential to said polysilicon gate, said second region and said silicon substrate; and

applying a forward bias ramping voltage between said diffused first region and said second region.

7. The method of claim 5, wherein

said diffused first region has a length of 50 to 100 microns and a width of 2 to 10 microns;

said polysilicon gate has a width of 0.5 to 1.5 microns; and

said polysilicon gate overlaps said diffused first region by 0.1 to 0.6 microns.

8. The method of claim 6, wherein said ground potential is zero volts, said ramping voltage is ramped from 0 to 0.85 and said pre-selected voltage is between 0.4 and 0.5 volts.

9. The method of claim 5 further comprising:

providing one or more STI-bounded reference diodes, said STI-bounded reference diodes each comprising a diffused

third region formed in an upper portion of a fourth region of said silicon substrate , said fourth region of an opposite dopant type from said diffused third region, said diffused third region surrounded by a peripheral dielectric isolation;

stressing each said STI-bounded reference diode;

measuring during said stressing, for each said STI-bounded reference diode, the current through said third diffused region as a function of said forward bias voltage applied between said third diffused region and said fourth regions at at least said predetermined forward bias voltage;

determining the frequency distribution of the slope of said forward bias voltage versus said diffused third region current at said pre-selected forward bias voltage for said one or more of STI-bounded reference diodes and

comparing said frequency distribution obtained from said STI-bounded reference diodes to said frequency distribution obtained from said polysilicon-bounded reference diodes.

10. A method for detecting semiconductor process stress-induced defects comprising:

providing one or more polysilicon-bounded test diodes, each polysilicon-bounded test diode comprising a diffused first region formed in an upper portion of a second region of a silicon substrate, said second region of an opposite dopant type from said diffused first region, said diffused first region surrounded by a peripheral dielectric isolation, a peripheral polysilicon gate comprising a polysilicon layer over a dielectric layer, said polysilicon gate overlapping a peripheral portion of said diffused first region;

stressing each said polysilicon-bounded test diode for a pre-determined amount of time; and

monitoring, after said stressing, each said polysilicon-bounded test diode for soft breakdown.

11. The method of claim 10, wherein said step of stressing comprises:

maintaining said polysilicon-bounded diode at an elevated temperature;

applying ground potential to said second region, said silicon substrate and said polysilicon gate; and

applying a fixed reverse bias voltage to between said first and second regions.

12. The method of claim 10, wherein

said diffused first region has a length of 50 to 100 microns and a width of 2 to 10 microns;

said polysilicon gate has a width of 0.5 to 1.5 microns; and

said polysilicon gate overlaps said diffused region by 0.1 to 0.6 microns.

13. The method of claim 11, wherein said ground potential is zero volts, said fixed voltage is between-6.3 and less than 0 volts, said fixed time is 0.5 hours or more and said elevated temperature is 100 to 200 °C.

14. A method for detecting semiconductor process stress-induced defects comprising:

providing a test DRAM, said test DRAM comprising a transfer device having a channel region between first and second P+ regions formed in a N-well in a silicon substrate and a gate formed over said channel region, said second P+ region electrically connected to a conductive core of a deep trench capacitor, said substrate acting as a second plate of said deep trench capacitor;

stressing said test DRAM; and

monitoring said stressed test DRAM for spikes in first P+ region current during said stressing.

15. The method of claim 14, wherein said step of stressing comprises:

maintaining said test DRAM at an elevated temperature;

applying ground potential to said N-well and said first P+ region;

applying a voltage to said gate sufficient to turn on said transfer device; and

applying a reverse bias ramping voltage to said silicon substrate.

16. The method of claim 15, wherein said ground potential is zero volts and said ramping voltage is ramped from 0 to -6 volts and said elevated temperature is 100 to 200 °C.

17. A method for detecting semiconductor process stress-induced defects comprising:

providing a test DRAM, said test DRAM comprising a transfer device having a channel region between first and second P+ regions formed in a N-well in a silicon substrate and a gate formed over said channel region, said second P+ region electrically connected to a conductive core of a deep trench capacitor, said substrate acting as a second plate of said deep trench capacitor;

stressing said test DRAM; and

monitoring said stressed test DRAM for spikes in gate current during said stressing.

18. The method of claim 17, wherein said step of stressing comprises:

maintaining said test DRAM at an elevated temperature;

applying ground potential to said N-well, said silicon substrate and said gate; and

applying a reverse bias ramping voltage to said first P+ region.

19. The method of claim 18, wherein said ground potential is zero volts and said ramping voltage is ramped from 0 to -6 volts and said elevated temperature is 100 to 200 °C.

20. A method for detecting semiconductor process stress-induced defects comprising:

providing a test DRAM, said test DRAM comprising a transfer device comprising a channel region between first and second P+ regions formed in a N-well in a silicon substrate and a gate formed over said channel region, said second P+ region electrically connected to a conductive core of a deep trench capacitor, said substrate acting as a second plate of said deep trench capacitor;

stressing said test DRAM;

measuring during said stressing, for said test DRAM, the current through said first P+ region as a function of a forward bias voltage applied between said first P+ region and said N-well at at least a pre-selected forward bias voltage; and

determining the frequency distribution of the slope of said forward bias voltage versus said first P+ region current at said pre-selected forward bias voltage for said one or more test DRAMs.

21. The method of claim 20, wherein said step of stressing comprises:

applying ground potential to said N-well and said silicon substrate;

applying a voltage to said gate sufficient to turn off said transfer device; and

applying a forward bias ramping voltage between said first P+ region and said N-well.

22. The method of claim 21, wherein said ground potential is zero volts and said ramping voltage is ramped from 0 to 0.85 and said pre-selected voltage is between 0.4 and 0.5 volts.

23. The method of claim 20 further comprising:

providing one or more reference devices, said reference devices each comprising a third P+ region formed in a N-well in said silicon substrate, said P+ region electrically connected to a conductive core of a deep trench capacitor, said substrate acting as a second plate of said deep trench capacitor;

stressing each said reference device identically to said test DRAM;

measuring during said stressing, for each said reference device, the current through said third P+ region

as a function of said forward bias voltage applied between said third P+ region and said N-well at at least said predetermined forward bias voltage;

determining the frequency distribution of the slope of said forward bias voltage versus said P+ region current at said pre-selected forward bias voltage for said one or more of reference devices; and

comparing said frequency distribution obtained from said reference devices to said frequency distribution obtained from said test DRAMs.

24. A method for detecting semiconductor process stress-induced defects comprising:

providing a test DRAM, said test DRAM comprising a transfer device comprising a channel region between first and second P+ regions formed in a N-well in a silicon substrate and a gate formed over said channel region, said second P+ region electrically connected to a conductive core of a deep trench capacitor, said substrate acting as a second plate of said deep trench capacitor;

stressing said test DRAM for a pre-determined amount of time; and

monitoring, after said stressing, each said test DRAM for soft breakdown.

25. The method of claim 24, wherein said step of stressing comprises:

maintaining said test DRAM at an elevated temperature;

applying ground potential to said first P+ region and said N-well;

applying a voltage to said gate sufficient to turn on said transfer device; and

applying a fixed reverse bias voltage to said silicon substrate; and

wherein said monitoring includes measuring a current through said first P+ diffusion as a function of time.

26. The method of claim 25, wherein said ground potential is zero volts, said fixed voltage is between-6.3 and 0 volts, said fixed time is 0.5 hours or more and said elevated temperature is 100 to 200 °C.

27. The method of claim 24, wherein said step of stressing comprises:

maintaining said test DRAM at an elevated temperature;

applying ground potential to said N-well, said gate and said substrate;

applying a fixed reverse bias voltage to said first P+ region; and

wherein said monitoring includes measuring a current through said gate as a function of time.

28. The method of claim 27, wherein said ground potential is zero volts, said fixed voltage is between-6.3 and less than

0 volts, said fixed time is 0.5 hours or more and said elevated temperature is 100 to 200 °C.

29. A method of fabricating an antifuse comprising:

providing a silicon substrate having a surface;

forming a ring of shallow trench isolation having an inner and an outer perimeter in said substrate extending from said surface of said substrate into said substrate;

forming a polysilicon gate overlapping said inner perimeter of said shallow trench isolation on said surface of said substrate, said polysilicon gate comprising a dielectric layer between said surface of said substrate and a polysilicon layer, said polysilicon gate having an inner and outer perimeter;

damaging said dielectric layer in a region along said inner perimeter of said polysilicon gate with a heavy ion specie implant to lower the breakdown voltage of said damaged dielectric layer in said region compared to the breakdown voltage in undamaged dielectric regions; and

forming a diffused region in said silicon substrate within the inner perimeter of said shallow trench isolation, said diffused region extending from said surface of said substrate into said substrate a depth not exceeding a depth of said shallow trench isolation.

30. The method of claim 29 wherein:

said diffused region has a length of 1 to 100 microns and a width of 1 to 10 microns;

said polysilicon gate has a width of 0.5 to 1.5 microns; and

said polysilicon gate overlaps said diffused region by 0.1 to 0.6 microns.

31. The method of claim 29 wherein said heavy ion specie is selected from the group consisting of germanium ion and arsenic ion.

32. The method of claim 29 further comprising forming a diffused-well of opposite polarity doping from said diffused region.

33. An antifuse comprising:

a silicon substrate having a surface;

a ring of shallow trench isolation having an inner and an outer perimeter in said substrate extending from said surface of said substrate into said substrate;

a polysilicon gate overlapping said inner perimeter of said shallow trench isolation on said surface of said substrate, said polysilicon gate comprising a dielectric layer between said surface of said substrate and a polysilicon layer, said polysilicon gate having an inner and outer perimeter;

a damaged region of said dielectric layer, said damaged region along said inner perimeter of said polysilicon gate, said damaged region damaged with a heavy ion specie implant and having a lower breakdown voltage than undamaged regions of said dielectric layer; and

a diffused region in said silicon substrate within the inner perimeter of said shallow trench isolation, said diffused region extending from said surface of said substrate into said substrate a depth not exceeding a depth of said shallow trench isolation.

34. The antifuse of claim 33 wherein:

said diffused region has a length of 1 to 100 microns and a width of 1 to 10 microns;

said polysilicon gate has a width of 0.5 to 1.5 microns; and

said polysilicon gate overlaps said diffused region by 0.1 to 0.6 microns.

35. The antifuse of claim 33 wherein said heavy ion specie is selected from the group consisting of germanium ion and arsenic ion.

36. The antifuse of claim 33 further comprising a diffused-well of opposite polarity doping from said diffused region.

37. The antifuse of claim 33 wherein a programming voltage of said antifuse voltage is dependent upon the area of said damaged region and independent of the area of said antifuse.

38. The antifuse of claim 33 wherein a programing voltage of said antifuse is a function of one or more of the group consisting of said heavy ion implant, the thickness of said

dielectric layer and a temperature of said antifuse when said programing voltage is applied.

39. The antifuse of claim 33 wherein the ratio of a resistance of said dielectric layer prior to application of a programing voltage to a resistance of said dielectric layer following application of said programming voltage is greater than 10^7.

40. The antifuse of claim 33 wherein the area of said antifuse is limited by the minimum critical dimension of the photolithographic system used to fabricate the antifuse.